## REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Claims 1-21 are all the claims pending in the application. Applicant submits the pending claims

define patentable subject matter.

### Claim Rejections - 35 USC § 102

Claims 1, 3, 4, 11, 13, 14, 18, 19 and 21 are rejected under 35 U.S.C. 102(b) as being

anticipated by Conley (US 2002/0099904).

In view of the above-noted amendments to claims 1 and 11, Applicant submits that

Conley fails to teach or suggest the claimed features, "wherein the flash memory state

information is written in a previous physical block[.]" Accordingly, Applicant submits that

independent claim 1 is patentable over Conley for at least these reasons. Similarly, Applicant

submits that independent claims 11 and 18 are patentable over Conley for analogous reasons.

Further, Applicant submits that claims 3, 4, 13, 14, 18, 19 and 21 are patentable over Conley, at

least by virtue of their dependency on claims 1, 11 and 18.

### Claim Rejections - 35 USC § 112

Claims 2, 12, 18 and 20 stand rejected under 35 U.S.C. §112, first paragraph, as failing to

comply with the enablement requirement. Specifically, the Examiner asserts that the claims

contain subject matter which was not described in the specification in such a way as to enable

one skilled in the art to which it pertains, or with which it is most nearly connected, to make

and/or use the invention.

Regarding claims 2, 12 and 20, the Examiner further states:

> [t]he Examiner is not aware of a portion of the specification which
> teaches how the meta-information is written after the data of the
> logical block is written. Accordingly, one of ordinary skill in the
> art would not know how to make or use the invention as recited in
> claims 2, 12, and 20.

In response, Applicant submits that the third full paragraph on page 10 of the

specification states: "[i]f atomicity for a write operation on a block basis is ensured, the data and

meta-information can be simultaneously written." In other words, if atomicity for a write

operation on a block basis is *not* ensured, the data and meta-information may be written in a way

other than simultaneously. Therefore, Applicant submits that the above-cited portion of the

specification would enable one skilled in the art to make and/or use the invention of claims 2, 12

and 20.

Applicant herein amends claim 18 to correct a typographical error. Specifically,

Applicant submits the phrase "wherein each physical block of the plurality of physical blocks

comprises a logical block number and flash memory state information comprising data and meta-

information" should instead read "wherein each physical block of the plurality of physical blocks

comprises data and meta-information, and the meta-information comprises a logical block

number and flash memory state information[.]"

In response to the Examiner's rejection of claims 18-21,[1] Applicant submits that the

enablement rejection is obviated by the correction of the typographical error noted above.

Claims 18-21 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply

with the written description requirement. Specifically, the Examiner asserts:

> [c]laim 18 recites the limitation "a first write operation which
> writes the data and the meta-information in a first physical block
> corresponding to the logical block number, if the first write
> operation has not previously been performed for the logical block
> number, and changes the flash memory state information." The
> Examiner is not aware of a portion of the specification that teaches
> that if a first write operation has not been previously been
> performed for the logical block, the controller changes the flash
> memory state information. It would seem that if there has not been
> a first write, there would be no flash memory state information to
> change.

Applicant respectfully disagree with the Examiner's rationale.

In response, Applicant submits that an example of the sufficiency of the written

description can be found in FIGS. 8a to 8c, and in the second full paragraph on page 14 of the

specification. In particular, Applicant points out that the above-noted paragraph states:

> [a] state value written in relevant LBN 3 in the BAT is investigated
> by using the read LBN 3.  <u>Since LBN 3 is a lower block that was
> accessed most recently, a state value has not been written and thus
> is "0."  Therefore, a state value of "1" is written in the relevant
> field of LBN 3 in the BAT (②).</u>[2]

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[1] Applicant notes that although paragraph 3 of the Office Action does not indicate claims 19-21 are
rejected under §112, first paragraph, as failing to comply with the enablement requirement, the
Examiner nevertheless indicates in paragraph 8 of the Office Action that claims 19-21 are also rejected
due to their dependency on claim 18.

[2] *See* specification, second full paragraph on page 14 (<u>emphasis</u> added).

In other words, according to this example, if a state value has not been previously been written for the logical block, the controller changes the flash memory state information from "0" to "1." Therefore, Applicant submits that the specification does support the above-noted features of the claim, and Applicant respectfully requests that the Examiner reconsider and withdraw the written description rejection of claims 18-21.

Claims 18-21 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for various informalities.

In response, Applicant herein amends independent claim 18 to address the informalities noted by the Examiner. Accordingly, Applicant submits that the indefiniteness rejection of claims 18-21 is obviated by our proposed clarifying amendment.

### *Claim Rejections - 35 USC § 103*

Claims 5, 6, 8-10, 15 and 17 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Conley in view of Kim et al. (US 6,381, 176; hereinafter "Kim").

Applicant submits that in view of the above-noted amendments to claims 1 and 11, Kim fails to cure the deficiency of Conley, as discussed above with regard to independent claim 1. Accordingly, Applicant submits that none of the cited references, either alone or in combination, teaches or suggests all of the claimed features of independent claims 1 and 11. Consequently, w Applicant submits that claims 5, 6, 8-10, 15 and 17 are patentable over the prior art of record, at least by virtue of their respective dependency on claims 1 and 11.

In view of the above, reconsideration and allowance of this application are now believed

to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is

kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue

Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any

overpayments to said Deposit Account.

Respectfully submitted,

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